What is claimed is:

1. A memory device having a plurality of memory cells, wherein each memory cell comprises a trench capacitor formed in a semiconductor substrate and an access transistor for it, wherein each access transistor comprises a first contact region connected to an internal electrode of the trench capacitor, a second contact region connected to a bit line and a control electrode region, wherein the control electrode regions of neighboring access transistors are connected by a word line formed in the semiconductor substrate.

2. The memory device according to claim 1, wherein the trench capacitor is formed in a trench in the semiconductor substrate, wherein the semiconductor substrate comprises a first region of a first conductivity type and an underlying second implanted region of a second conductivity type, wherein the trench of the memory cell extends over the first and second regions.

3. The memory device according to claim 1, wherein the access transistor is a field effect transistor having a channel region, wherein the control electrode region of the access transistor has an oxide layer separating the channel region of the access transistor from the control electrode region.

4. The memory device according to claim 3, wherein the layer thickness of the control electrode oxide layer is in a range of 0.5 to 15 nm and is preferably in a range of 3 to 6 nm.

5. The memory device according to claim 3, wherein the control electrode oxide layer comprises an SiO_2 material.

6. The memory device according to claim 1, wherein the access transistor is a vertical field effect transistor.

7. The memory device according to claim 6, wherein the channel region of the vertical field effect transistor is formed in the trench of the memory cell.

8. The memory device according to claim 6, wherein the control electrode region completely surrounds the channel region of the access transistor.

9. The memory device according to claim 1, wherein the access transistor is a tunnel transistor.

10. The memory device according to claim 1, wherein the word line is a highly doped region buried in the semiconductor substrate.

11. The memory device according to claim 10, wherein the word line is a highly doped region of the second conductivity type completely formed in the first region of the semiconductor substrate and surrounded by it, and is isolated from the second region by the first region.

12. The memory device according to claim 10, wherein the highly doped word line region is connected to the control electrode region of the access transistor.

13. The device according to claim 11, wherein the first region, the second underlying region and the highly doped word line region are formed by means of implantation in the semiconductor substrate.

14. The memory device according to claim 1, wherein the highly doped word line region can be contacted outside the memory cell.

15. The memory device according to claim 1, wherein a plurality of memory cells can be combined to a memory cell field.

16. The memory device according to claim 1, wherein the first conductivity type is a p conductivity type and the second conductivity type is an n conductivity type.

17. The memory device according to claim 1, wherein the first conductivity type is an n conductivity type and the second conductivity type is a p conductivity type.

18. A method of manufacturing a memory device having a plurality of memory cells, comprising the following steps:

providing a semiconductor substrate;

forming a trench in the semiconductor substrate;

forming a signal memory capacitor in the trench in the semiconductor substrate;

forming an access transistor above the signal memory capacitor in the trench, wherein the access transistor has a first contact region connected to an internal electrode of the signal memory capacitor, a second contact region connected to a bit line and a control electrode region; and

forming a highly doped word line region in the semiconductor substrate, wherein the control electrode region of the access transistor is connected to the highly doped word line region.

19. The method according to claim 18, wherein the step of forming the access transistor further comprises the following steps:

growing a thermal control electrode oxide;

exposing a contact to the internal electrode of the signal memory capacitor by means of etching;

filling the trench with a metal material;

selectively etching the metal material back to obtain the metal region;

performing an oxidation on the metal region to obtain an oxide layer; and

filling the trench with a metal material in order to obtain another metal region.

20. The method according to claim 18, wherein the step of forming the signal memory capacitor further comprises the following steps:

implanting a first region of a first conductivity type in the semiconductor substrate; and

implanting an underlying second region of a second conductivity type in the semiconductor substrate.

21. The method according to claim 18, wherein the step of forming the highly doped word line region further comprises the following steps:

depositing a mask on the semiconductor substrate to define regions in which the buried word line region is to be formed;

implanting a doping material into the semiconductor substrate to form the buried word line region;

oxidizing the substrate surface to obtain a surface oxidation layer; and

contact-etching through the surface oxidation layer to the metal regions.

22. The method according to claim 18, wherein the metal comprises an Nb material and/or Ti material.

23. The method according to claim 18, wherein the memory device is a DRAM memory device.